Abstracts

A Double-Polysilicon Bipolar Process with a 0.3-µm Minimum Emitter Width and NMOS Transistors for Low Power Wireless Applications

K. O, C. Tsai, T. Tewksbury, G. Dawe, C. Kermarrec and J. Yasaitis. "A Double-Polysilicon Bipolar Process with a 0.3-µm Minimum Emitter Width and NMOS Transistors for Low Power Wireless Applications." 1995 MTT-S International Microwave Symposium Digest 95.2 (1995 Vol. II [MWSYM]): 531-534.

A 0.6-µm 3.5-V silicon bipolar process is developed for low power and high speed operation in wireless applications. The process features 35-GHz f/sub T/ bipolar transistors with a 0.3-µm electrical emitter width, lateral pnp transistors, polysilicon-to-n/sup +/ plug capacitors, NMOS transistors with a 10-nm gate oxide layer for low on-resistance, and inductors fabricated using a double level metal process. Improvement of the low power and high speed performance of the npn transistors is demonstrated by examining the trade-offs among r/sub b/+r/sub e/, collector current required to achieve a fixed f/sub T/, and device geometry. Microwave and RF capabilities are demonstrated by fabricating and characterizing low noise amplifiers and NMOS transistors.

❑ Return to main document.